Amendments to the Specification:

Please amend the paragraph beginning on page 5, line 9 as follows:

--A silicon substrate ~~100~~ 10 may be single-crystal silicon or an epitaxial silicon layer formed on a single crystal substrate is shown in Figure 2A ~~1~~. This substrate may contain any number of integrated circuit devices such as transistors, diodes, etc., which all form part of the integrated circuit. ~~This~~ These devices are omitted from Figures 2A – 2F for clarity. Following the fabrication of such devices, a first intra-metal-dielectric (IMD) layer 30 is formed on the substrate 10 and copper metal layers 40 and 50 are formed in the IMD layer 30. Typically, these copper layers 40, 50 are formed using a damascene process. In the damascene process a trench is first formed in the IMD layer 30. A trench liner/barrier film is then formed in the trench followed by copper deposition. The trench liner usually comprises a tantalum nitride film with typical field thickness on the order of 100A – 2000A. Following copper film formation, which completely fills the trench, chemical mechanical polishing (CMP) is performed to remove the excess copper and produce the copper layers 40 and 50 whose top surfaces are planar with the surface of the IMD layer 30 as shown in Figure 2A. The copper layer 40 will function as one plate of a capacitor structure and 50 is part of the metal interconnect structure associated with a metal level or layer in the integrated circuit.--